Amendments to the Claims

The listing of claims below will replace all prior versions and listings of claims in the application.

1-7. (Cancelled)

8. (Currently Amended) ~~Simulation~~ A simulation system for ~~simulation~~ simulating a response of an electronic circuit, the circuit being representable by a network of logical elements, comprising:

a first asynchronous clock domain; and

a second asynchronous clock domain, coupled to the first asynchronous clock domain, including ~~one or more jitter elements~~ a first jitter element and a second jitter element, wherein ~~at least one of the one or more jitter elements is~~ the first jitter element includes a delay element and a multiplexer, the first jitter element being configured to randomly introduce predetermined timing delays into data from the first asynchronous clock domain, the first jitter element being insertable in the second asynchronous clock domain at a circuit boundary between the first asynchronous clock domain and the second asynchronous clock domain, and the second jitter element includes an x generator element configured to randomly introduce predetermined signal values into the data from the first asynchronous clock domain.

9. - 11. (Cancelled)

12. (Currently Amended) The system of claim 8, wherein [[the]] at least one of ~~the one or more jitter elements are~~ the first jitter element and the second jitter element is interactively inserted by a user.

13. (Currently Amended) The system of claim 8, wherein [[the]] at least one of ~~the one or more jitter elements are~~ the first jitter element and the second jitter element is configured to be automatically inserted using predetermined modules.

14-15. (Cancelled)

16. (Currently Amended) The system of claim 8, wherein ~~the one or more jitter elements are~~ at least one of the first jitter element and the second jitter element is representable as logical elements, the values of which are randomly set.

17. (Cancelled)

18. (Currently Amended) An electronic circuit representable by a network of logical elements, comprising:

a first asynchronous clock domain; and

a second asynchronous clock domain, coupled to the first asynchronous clock domain, including ~~one or more jitter elements~~ a first jitter element and a second jitter element, wherein ~~at least one of the one or more jitter elements is~~ the first jitter element includes a delay element and a multiplexer, the first jitter element being configured to randomly introduce predetermined timing delays into data from the first asynchronous

clock domain, the first jitter element being insertable in the second asynchronous clock domain at a circuit boundary between the first asynchronous clock domain and the second asynchronous clock domain, and the second jitter element includes an x generator element configured to randomly introduce predetermined signal values into the data from the first asynchronous clock domain.

19. - 20. (Cancelled)

21. (Currently Amended) The circuit of claim 18, wherein [[the]] at least one of ~~the one or more jitter elements are~~ first jitter element and the second jitter element is interactively inserted by a user.

22. (Currently Amended) The circuit of claim 18, wherein [[the]] at least one of ~~the one or more jitter elements are~~ first jitter element and the second jitter element is configured to be automatically ~~inserted~~ insertable using predetermined modules.